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Introducing the Xilinx Targeted Design Platform: Fulfilling the Programmable Imperative

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For two-and-a-half decades, Xilinx has been at the forefront of the programmable logic revolution, with the invention and continued migration of FPGA platform technology. During that time, the role of the FPGA has evolved from a vehicle for prototyping and glue-logic to a highly flexible alternative to ASICs and ASSPs for a host of applications and markets.

Today, Xilinx® FPGAs have become strategically essential to world-class system companies that are hoping to survive and compete in these times of extreme global economic instability, turning what was once the programmable revolution into the "programmable imperative" for both Xilinx and our customers.

The Programmable Imperative

When viewed from the customer's perspective, the programmable imperative is the necessity to do more with less, to remove risk wherever possible, and to differentiate in order to survive. In essence, it is the quest to simultaneously satisfy the conflicting demands created by ever-evolving product requirements (i.e., cost, power, performance, and density) and mounting business challenges (i.e., shrinking market windows, fickle market demands, capped engineering budgets, escalating ASIC and ASSP non-recurring engineering costs, spiraling complexity, and increased risk).

To Xilinx, the programmable imperative represents a two-fold commitment. The first is to continue developing programmable silicon innovations at every process node that deliver industry-leading value for every key figure of merit against which FPGAs are measured: price, power, performance, density, features, and programmability. The second commitment is to provide customers with simpler, smarter, and more strategically viable design platforms for the creation of world-class FPGA-based solutions in a wide variety of industries—what Xilinx calls *targeted design platforms*.

Xilinx targeted design platforms provide the optimum in flexibility, accessibility, applicability, and time to market. A brief look at the three strata into which the targeted design platforms are organized reveals how Xilinx has accomplished this (see Figure 1).

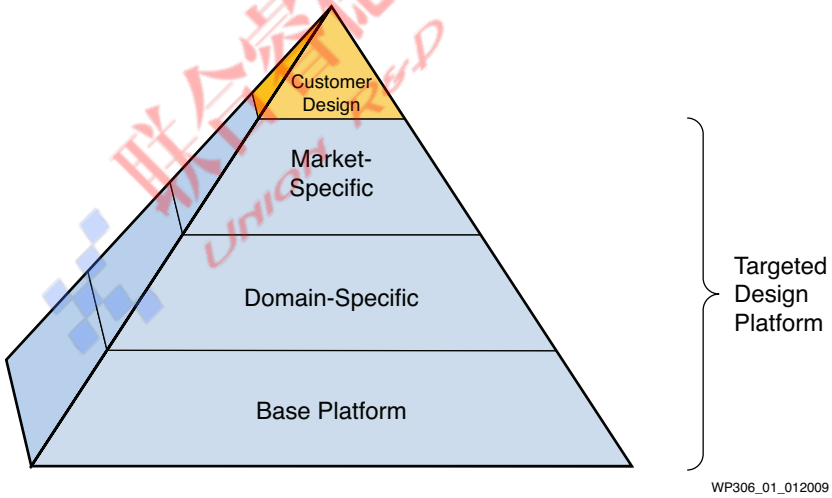

Figure 1: **Targeted Design Platform**

Xilinx targeted design platforms accelerate the customers' design cycles and enable them to spend less time developing the infrastructure of an application and more time creating their unique value in the design.

Base Platform

The base platform is both the delivery vehicle for all new silicon offerings from Xilinx *and* the foundation upon which all Xilinx targeted design platforms are built. As such, it is the most fundamental platform used to develop and run customer-specific software applications and hardware designs as production system solutions.

Released at launch, the base platform comprises a robust set of well-integrated, tested, and targeted elements that enable customers to immediately start a design. These elements include:

- FPGA silicon
- ISE® Design Suite design environment
- Third-party synthesis, simulation, and signal integrity tools
- Reference designs common to many applications, such as memory interface and configuration designs
- Development boards that run the reference designs
- A host of widely used IP, such as GigE, Ethernet, memory controllers, and PCIe®.

Domain-Specific Platform

The next layer in the targeted design platform hierarchy is the domain-specific platform. Released from three to six months after the base platform, each domain-specific platform targets one of the three primary Xilinx FPGA user profiles (domains): the embedded processing developer, the digital signal processing (DSP) developer, or the logic/connectivity developer. This is where the real power and intent of the targeted design platform begins to emerge.

Domain-specific platforms augment the base platform with a predictable, reliable, and intelligently targeted set of integrated technologies, including:

- Higher-level design methodologies and tools
- Domain-specific *embedded*, *DSP*, and *connectivity* IP
- Domain-specific development hardware and daughter cards
- Reference designs optimized for embedded processing, connectivity, and DSP
- Operating systems (required for embedded processing) and software

Every element in these platforms is tested, targeted, and supported by Xilinx and/or our ecosystem partners. Starting a design with the appropriate domain-specific platform can cut weeks, if not months, off of the user's development time.

Market-Specific Platform

A market-specific platform is an integrated combination of technologies that enables software or hardware developers to quickly build and then run their specific application or solution. Built for use in specific markets such as Automotive, Consumer, Mil/Aero, Communications, AVB, or ISM, market-specific platforms integrate both the base and domain-specific platforms and provide higher level elements that can be leveraged by customer-specific software and hardware designs.

The market-specific platform can rely more heavily on third-party targeted IP than the base or domain-specific platforms. The market-specific platform includes: the base and domain-specific platforms, reference designs, and boards (or daughter cards) to

run reference designs that are optimized for a particular market (e.g., lane departure early-warning systems, analytics, and display processing).

Xilinx will begin releasing market-specific platforms three to six months after the domain-specific platforms, augmenting the domain-specific platforms with reference designs, IP, and software aimed at key growth markets. Initially, Xilinx will target markets such as Communications, Automotive, Video, and Displays with platform elements that abstract away the more mundane portions of the design, thereby further reducing the customer's development effort so they can focus their attention on creating differentiated value in their end solution.

This systematic platform development and release strategy provides the framework for the consistent and efficient fulfillment of the programmable imperative—both by Xilinx and by its customers.

Platform Enablers

Xilinx has instituted a number of changes and enhancements that have contributed substantially to the feasibility and viability of the targeted design platform. These *platform-enabling* changes cover six primary areas:

- Design environment enhancements
- Socketable IP creation
- New *targeted* reference designs
- Scalable unified board and kit strategy
- Ecosystem expansion
- Design services supporting the targeted design platform approach

Design Environment Enhancements

With the breadth of advances and capabilities that the Virtex®-6 and Spartan®-6 programmable devices deliver coupled with the access provided by the associated targeted design platforms, it is no longer feasible for one design flow or environment to fit every designer's needs. System designers, algorithm designers, SW coders, and logic designers each represent a different user-profile, with unique requirements for a design methodology and associated design environment. Instead of addressing the problem in terms of individual fixed tools, Xilinx targets the required or preferred methodology for each user, to address their specific needs with the appropriate design flow. At this level, the design language changes from HDL (VHDL/Verilog) to C, C++, MATLAB® software, and other higher level languages which are more widely used by these designers, and the design abstraction moves up from the block or component to the system level. The result is a methodology and complete design flow tailored to each user profile that provides design creation, design implementation, and design verification.

Indicative of the complexity of the problem, to fully understand the user profile of a "logic designer," one must consider the various levels of expertise represented by this demographic. The most basic category in this profile is the "push-button user" who wants to complete a design with minimum work or knowledge. The push-button user just needs "good-enough" results. Contrastingly, more advanced users want some level of interactive capabilities to squeeze more value into their design, and the "power user" (the expert) wants full control over a vast array of variables. Add the traditional ASIC designers, tasked with migrating their designs to an FPGA (a growing trend, given the intolerable costs and risks posed by ASIC development these

days), and clearly the *imperative* facing Xilinx is to offer targeted flows and tools that support each user's requirements and capabilities, on their terms.

The most recent release of the ISE Design Suite includes numerous changes that fulfill requirements specifically pertinent to the targeted design platform. The new release features a complete tool chain for each top-level user profile (the domain-specific personas: the embedded, DSP, and logic/connectivity designers), including specific accommodations for everyone from the push-button user to the ASIC designer. The tighter integration of embedded and DSP flows enables more seamless integration of designs that contain embedded, DSP, IP, and user blocks in one system.

To further enhance productivity and help customers better manage the complexity of their designs, the new ISE Design Suite enables designers to target area, performance, or power by simply selecting a design goal in the setup. The tools then apply specific optimizations to help meet the design goal. In addition, the ISE Design Suite boasts substantially faster place-and-route and simulation run times, providing users with 2X faster compile times. Finally, Xilinx has adopted the FLEXnet Licensing strategy that provides a floating license to track and monitor usage.

Socketable IP

Xilinx has coined the term *socketable IP* to refer to IP that customers can easily use without the need for significant support, i.e., plug-and-play IP. Xilinx started developing IP long before there were defined standards to make IP plug-and-play capable. However, over the last 10 years as the IP industry has matured, companies with large repositories of IP have begun looking seriously for ways to preserve and extend this huge investment. To accomplish these objectives, one of the standards adopted by the IP industry is IP-XACT. Xilinx is moving to this industry-standard repository format with the goal of opening CORE Generator™ software, included in the ISE Design Suite, to third-party and customer IP for design reuse. CORE Generator software provides a catalog of user-customizable functions ranging in complexity from commonly used functions such as memories and FIFOs, to system-level building blocks such as filters and transforms.

In addition, Xilinx has adopted and extended the proposed IEEE standard for IP Quality (QIP) and is using this on IP we develop as well as the IP of our ecosystem partners. As an industry leader, Xilinx long ago had to develop and provide a proprietary encryption methodology and is the only FPGA vendor targeted to deliver secure solutions for domestic U.S. government specifications. Xilinx is now leveraging this knowledge to help drive IEEE standards (IEEE Std 1735). When ratified, the standard will enable Xilinx to simplify and secure all socketable IP in its repository, regardless of who developed it.

Targeted Reference Designs

Xilinx has aligned reference design development and delivery with our robust third-party ecosystem by defining a new class of reference design called the *targeted reference design*. Targeted reference designs meet requirements that are above and beyond standard reference designs. While Xilinx will continue to support many standard reference designs (see Table 1), targeted reference designs are built with standard IP components and framework guaranteed for use with specified silicon and are fully verified, validated, and supported throughout the product life-cycle.

The impact of this particular innovation will ripple up through every layer of the targeted design platform by providing a common starting point for multiple domains,

addressing different user profiles. Thus, the new base platform will provide greater interoperability and ease of use for all domains.

Table 1: **Reference Design Standards Matrix**

Reference Design Standards	Legacy	Standard	Targeted
Available on xilinx.com	3	3	3
Targets latest Xilinx devices (e.g., Virtex-6 and Spartan-6 FPGAs)		3	3
Verified and validated		3	3
Support and upgrades commitment			3
Integrates multiple building blocks			3
Scalable to include user logic			3
Uses best-in-class targeted IP			3

Unified Board Strategy

The Virtex-6 and Spartan-6 families mark the release of a new unified board strategy that enables the efficient creation of a standardized and coordinated set of base boards available both from Xilinx and our ecosystem partners. These scalable and flexible base boards all utilize the industry-standard FPGA mezzanine card (FMC) for daughter card extensions (see Figure 2). Sponsored by VITA, the FMC (VITA 57) standard was developed with the FPGA in mind and is supported by a growing list of silicon, board, and system companies. Adopting this standard for all of our base boards enables the creation of a unified, scalable, and extensible delivery mechanism for all Xilinx targeted design platforms.

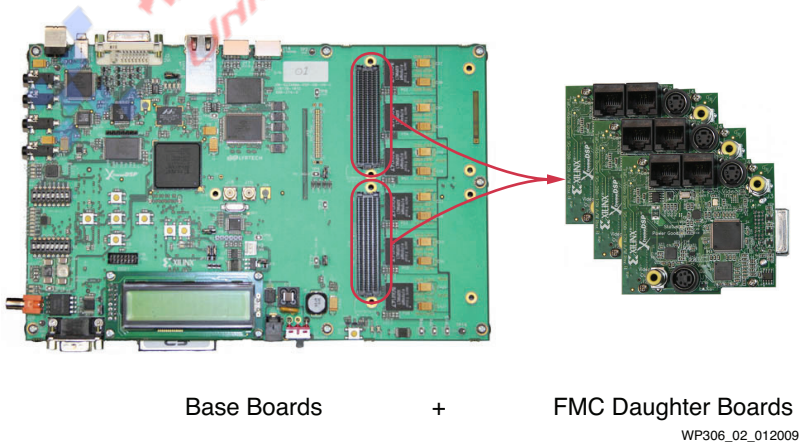

Figure 2: **Flexible Interconnect between the Card and the FPGA**

Ecosystem Expansion

Over the past few decades, Xilinx and our partners have developed a robust ecosystem of IP, boards, tools, services, and support through the Xilinx alliance partners program. Moving forward with these alliance partners, targeted design platforms will be extensible through third-party IP, software, boards, and design services, and leveraged in customer designs. To facilitate the integration of the ecosystem products into design platforms, Xilinx is transitioning from what has been historically a closed platform approach to an open platform approach. Specifically, Xilinx is moving to industry standards and interfaces. In the IP area, Xilinx is moving

to interconnect standards, IP repository standards, and industry-standard encryption methods. Xilinx will also define and open application programming interfaces (APIs) to facilitate the adoption of third-party tools into a user's flow, enabling the user to benefit from best-in-class design creation, verification, and implementation tools.

These changes provide significant benefits to designers and the Xilinx third-party alliance members, by enabling them to more easily integrate their products and services into a standardized development, integration, and delivery methodology. These changes will result in greater development efficiencies for both the third-party alliance members and our mutual customers.

Engineering Services

Xilinx engineering services and targeted third-party alliance member services enhance targeted design platforms by allowing the customer to focus even more on their core competencies, realize additional time-to-market efficiencies, and reduce their fixed engineering costs. These services provide customers with engineering resources to augment their design team and to provide expert design-specific advice. Xilinx tailors its engineering services to the needs of its customers, ranging from hands-on training to full design creation and implementation.

Specifically, Xilinx engineering services include Xilinx Design Services, Titanium Dedicated Engineering, and QuickStart! Xilinx Design Services provides FPGA design specialists that can execute part or all of a customer's design. This veteran team provides our customers with turn-key custom development that focuses on project design and management. Titanium Dedicated Engineering provides the customer with dedicated FPGA expertise and is an onsite engineering resource focused at the base and domain-specific levels of the targeted design platform (e.g., providing FPGA embedded expertise). QuickStart! is an up-front customized service option that provides the customer with two days of specialized training and three days of hands-on technical advice, and supports a customer's design with a variety of offerings targeted at the base and domain-specific levels of the targeted design platform.

Targeted Design Platform at Work

Example: Spartan-3A DSP FPGA Video Starter Kit (Available Now)

Xilinx has successfully tested a subset of the targeted design platform concept with the introduction of the Spartan-3A DSP FPGA and the Video Starter Kit. The Spartan-3A DSP FPGA Video Starter Kit is built upon a base platform that includes a Spartan-3A DSP XC3SD3400A FPGA and base IP. To this, Xilinx adds domain specific elements, such as an FMC-Video I/O daughter card, a CMOS camera module, and a comprehensive set of Xilinx development tools that include a one-year entitlement for the Embedded Development Kit and System Generator for DSP. To accelerate development, this market-specific platform includes video reference designs built around an embedded design framework that the user can quickly and easily customize to include video pipeline blocks. Using the set of reference designs as starting points, users can get customized video designs running within hours. In addition, customers can also accelerate their development effort by drawing from the extensive Xilinx library of horizontal IP and reference designs and include them within the framework of the base reference design provided with the kit.

This same approach, which will be applied to all new product families, including Spartan-6 and Virtex-6 FPGAs, exemplifies the value of the targeted design platform,

enabling customers to begin working on their particular applications without having first developed a hardware board or basic designs and framework just to get started.

Summary

To be truly agile, today's development teams need new methodologies that support their tight development cycles, even tighter budgets, and relentlessly increasing product and technological complexity. The simultaneous introduction of the Virtex-6 and Spartan-6 families and the new targeted design platform strategy marks a major inflection point in a long-term commitment by Xilinx to aid our customers in their quest to fulfill the programmable imperative.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/02/09	1.0	Initial Xilinx release.
06/24/09	1.1	Updated for ISE Design Suite 11.2.

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